REMARKS

Claims 1-29 are pending. Claims 1, 12 and 13 have been amended. No new matter is presented.

Claim 7 was objected to because the Examiner believes that it is unclear how the testing time frame is determined less than two seconds after loading of the carrier with the semiconductor chip. The Examiner asks what device is used to determine the time frame. Applicant respectfully traverses this objection.

Applicant is not intending to claim a timing device, but merely trying to claim a time frame in which the testing begins after the carrier is loaded with the semiconductor chip. Thus, it is not necessary for applicant to recite a specific structure for timing the testing. Accordingly, withdrawal of this objection is requested.

The objection to claim 13 has been overcome by amendment.

Claims 1-24, 26, 28-29 stand rejected under 35 USC 102(b) as being anticipated by Matsuda, U.S. Patent 4,730,156. Claims 25 and 27 are rejected under 35 USC 103(a) as being unpatentable over Matsuda in view of Farnworth, U.S. Patent 6,369,595. These rejections are respectfully traversed.

Claim 1 recites "[A] testing method for testing contacting between a semiconductor chip and a test carrier." Matsuda fails to teach or suggest this feature.

Instead, Matsuda teaches a method for testing a contact between an IC package and a printed circuit board (see column 1, lines 8 - 11: "microprocessor which generates an alarm when an IC package ... is erroneously connected to a printed circuit board", column 1, lines 12 - 14: "self-check ... confirming accurate connection of the IC package to the printed circuit board", column 1, lines 49 - 51: "detect erroneous connection of the IC package to a printed circuit board", column 2, lines 63 - 64, etc.).

The IC packages 10a /IC sockets 16a shown e.g. in Figure 2 (see e.g. column 2, lines 45 - 49, etc.) of Matsuda do not correspond to the claimed test carriers, but are one and the same IC packages l0a /IC sockets 16a as used during ordinary operation of the system (see e.g. column 1, lines 9 - 11, etc.).

Further, Matsuda does not teach or suggest that the contacting between a test carrier and a semiconductor chip is tested *immediately after* the loading of the test carrier with the semiconductor chip, as recited in amended claims 1 and 12.

Matsuda likewise fails to teach or suggest that a "semiconductor chip comprises one or more contacting test contacts exclusively for testing the contacting between the semiconductor chip and the test carrier immediately after the loading of the test carrier with the semiconductor chip." Rather, Matsuda teaches the opposite, testing the contacting during a "cold-start" of a printed circuit board (see column 1, lines 12 - 14: "self-check during so-called "cold start" confirming accurate connection of the IC package to the printed circuit board").

Hence, before the contacting is tested, according to Matsuda, i) a "blank" chip is mounted into an IC package 10a, and ii) the IC package l0a is mounted to a printed circuit board, and ill) a "cold start" has to be performed.

Therefore, Matsuda does not teach or suggest the features of claims 1 or 12. The remaining claims are allowable at least due to their respective dependencies and further in view of Farnworth's failure to overcome the deficiencies of Matsuda.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue. If it is determined that a telephone conference would expedite the prosecution of this application, the Examiner is invited to telephone the undersigned at the number given below.

In the event the U.S. Patent and Trademark office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to Deposit Account No. 03-1952 referencing docket no. 543822002400.

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Respectfully submitted,

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